REMARKS

Claims 1, 18, 20, 30, 37, 56, and 65 have been amended. No claims have been canceled. No new claims have been added. Claims 1-69 are pending.

Claims 65-66 and 69 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Houg (U.S. Patent No. 6,322,596). Claims 67-68 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Houg. Claims 1-35, 37-46, and 48-63 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Blackmon (U.S. Patent No. 6,513,091) in view of Houg. Claims 36 and 47 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Blackmon in view of Houg. Claims 65-69 stand rejected as being unpatentable over Blackmon. These rejections are respectfully traversed.

Independent claims 1, 18, 20, and 30 are each directed to methods for transferring data in a system which includes a link bus. As recited in claims 1, 18, 20, and 30, the link bus comprises: "a hub device and a plurality of link bus segments each comprising a plurality of lines for communicating commands, addresses, and data, and a status line, each link bus segment being coupled to said hub device and one respective satellite device of said link bus to form a point-to-point link between said hub and respective satellite device, one of said respective satellite device being a first device, a processor coupled to said hub device via by a processor bus device coupled to said hub device via a memory bus."

Each one of claims 1, 18, 20, and 30 further recite the steps of obtaining or driving status information from the status line of the link bus. More specifically:

> Claim 1 recites, *inter alia*, "obtaining a status of the request by observing the status line of said link bus during a first predetermined window of time; ...

obtaining a status of the initiated transfer by observing the status line of said link bus during a second predetermined window of time";

Claim 18 recites, *inter alia,* "driving the status on the status line of said link bus during a first predetermined window of time, ... obtaining a status of an initiated transfer of data over said link bus by observing the status line of said link bus during a second predetermined window of time";

Claim 20 recites, *inter alia,* "driving the status on the status line of said link bus during a first predetermined window of time, ... obtaining a status of an initiated transfer of data over said link bus by observing the status line of said link bus during a second predetermined window of time"; and

Claim 30 recites, *inter alia,* "driving the status of the data transfer on the status line of said link bus during a first predetermined window of time; obtaining the status of the transfer by observing the status line of said link bus during the first predetermined window of time."

Additionally, each one of method claims 1, 18, 20, and 30 further recite limitations directed to stalling a data transfer on the link bus. More specifically:

Claim 1 recites, *inter alia,* "determining from the obtained transfer status whether the initiated data transfer should be stalled";

Claim 18 recites, *inter alia,* "if it is determined that the initiated transfer should be stalled, driving a stalled status indication on the status line of said link bus during a second predetermined window of time and stalling the transfer";

Claim 20 recites, *inter alia,* "determining from the obtained transfer status whether the initiated data transfer should be stalled"; and

Claim 30 recites, *inter alia*, "if it is determined that the initiated transfer should be stalled, driving a stalled status indication on the status line of said link bus during a second predetermined window of time and stalling the transfer."

Claims 37, 56, and 65 are apparatus claims, and recite limitations similar to the above quoted portions of method claims 1, 18, 20, and 30. More specifically:

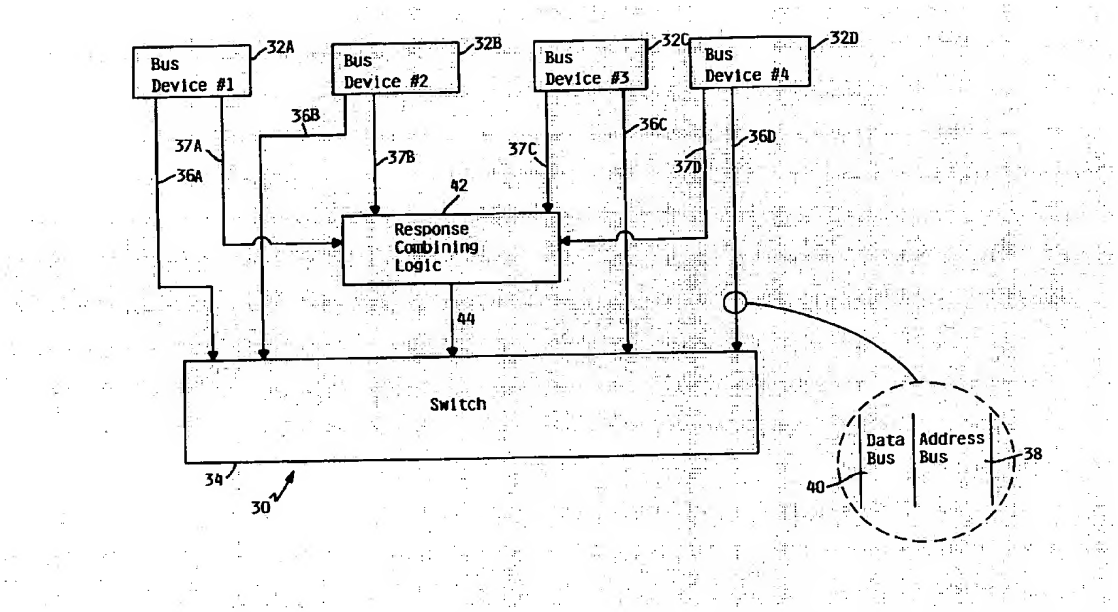
Claim 37 recites, *inter alia*: "A processor system comprising: ... a link bus, said link bus comprising, a link hub, said link hub being connected to said processor via a processor bus; a plurality of link bus segments, each comprising a first bus for communicating commands, addresses, and data, and a status line, each link bus segment being coupled to said hub device and one device of said link bus to form a point-to-point link directly connecting said hub and respective link bus device, one of said respective link bus devices being a satellite device; ... wherein one of said link hub and said satellite device is a bus master and the other of said link hub and satellite device is a target; said master issues a data transfer request on said first bus, obtains a status of the request by observing said status line of said link bus during a first predetermined window of time, ... obtains a status of the initiated transfer by observing said status line of said link bus during a second predetermined window of time, and determines from the obtained transfer status whether the initiated data transfer should be stalled."

Claim 56 recites, inter alia, "A processor system comprising: ... a link bus, said link bus comprising, a link hub connected to said processor via a processor bus; and a plurality of link bus segments, each comprising a first bus for communicating commands, addresses, and data, and a status line, each link bus segment being coupled to said hub device and one device of said link bus to form a point-to-point link directly connecting said hub and respective link bus

device, one of said respective link bus devices being a satellite device; wherein one of said link hub and said satellite device is a bus master and the other of said link hub and satellite device is a target; ... drives the status on said status line of said link bus during a first predetermined window of time, ... said target obtains a status of an initiated transfer of data over said link bus by observing said status line of said link bus during a second predetermined window of time, and determines from the obtained transfer status whether the initiated data transfer should be stalled"; and

Claim 65 recites, *inter alia,* "A processor system comprising: ... a link bus, said link bus comprising, a link hub connected to said processor via a processor bus; and a plurality of link bus segments, each comprising a first bus for communicating commands, addresses, and data, and a status line, each link bus segment being coupled to said hub device and one device of said link bus to form a point-to-point link directly connecting said hub and respective link bus device, one of said respective link bus devices being a satellite device; wherein one of said link hub and said satellite device is a bus master and the other of said link hub and satellite device is a target; and said master and target being able to at least initiate, disconnect, retry, abort and stall data transfers on said first bus by time multiplexing disconnecting and pacing status information on said status line."

Referring to Fig. 1 (reproduced below), Blackmon discloses a data routing method and apparatus in a system comprising a data/address bus 36, a switch 34, and a network of status response signals 37, 42, 44. In Blackmon's system, bus devices 32A-32D, referred to collectively as 32, are coupled to a bus 36.



The bus 36 is a plurality of point-to-point connections 36A-36D, and is used to directly couple and permit communication of address and data between each bus device 32 and the switch 34. Communication between bus devices take place via the switch 34. Significantly, Blackmon also discloses using a status network comprising status lines 37A-37D (collectively referred to as 37). The status lines 37 are coupled to a response combining logic 42, which is itself coupled via link 44 to the switch 34.

Fig. 3 illustrates a system substantially similar to the system illustrated in Fig. 1. The Fig. 3 system differs from the Fig. 1 system by including more devices in the system. Referring to Fig. 3, the Final Rejection asserts that Blackmon discloses a processor system comprising a processor 72, 74, 78, a link hub 42 connected to the processor via a processor bus 104, 106, 108, 110, 116, 118, a satellite device 76, 80, 82, and a link bus 112, 114, 120, 122, 124, 126. The link bus is said to be directly connected between the link hub 42 and the satellite devices 76, 80, 82. The link bus 42 is asserted to include a status line and a first bus.

It is respectfully asserted that the Final Rejection is in error. For example, the Final Rejection alleges that Blackmon discloses the claimed link bus as links 112, 114, 120, 122, 124, and 126 with the response combining logic 42 as the link hub. However, the links 112, 114, 120, 122, 124, and 126 cannot be the link bus and the response combining logic cannot be the claimed link hub, because links 112, 114, 120, 122, 124, and 126 are links for conveying only status information between the bus devices the response combining logic 42. Independent method claims 1, 18, 20, 30 are directed to methods for transferring data on a link bus, while independent apparatus claims 37, 56, and 65 are directed to systems for transferring data on a link bus. In contrast, the links 112, 114, 120, 122, 124, and 126 identified by the Final Rejection do not transfer data. Accordingly, for this reason alone they cannot be the claimed link bus.

Further, as recited in the independent claims, the link bus is required to include a status line, and the link bus is required to be directly coupled to the link hub. Fig. 3 illustrates a plurality of links for transferring data and addresses (e.g. links 88, 90, 92, 96) which are directly connected between respective bus devices and the switch 34, but none of the status lines (i.e., links 112, 114, 120, 122, 124, and 126) are directly connected to the switch 34. In fact, the bus architecture of Blackmon is fundamentally different from the claimed invention because Blackmon's bus architecture separates the status lines from the command/address lines. In Blackmon's system, all status information is routed on a separate bus system which is independent of the command/address links which form the command/address bus. The response combining logic 42 serves as an interface between the status bus links and the address/command bus links. None of the status bus links are directly connected to the same hub as all of the command/address links.

Further, each independent claim also recite limitations directed to stalling a data transfer which has already been initiated. With respect to "stalling," the Final

Rejection states at pages 5-6 "[t]he AStatOut/AStatIn status response signals 37 provide a positive acknowledgment of an address being accepted by a bus device, a null response (stall), or an indication that the transaction should be terminated immediately (i.e., address parity error or retry)." It is respectfully asserted that the Final Rejection is in error.

The "stalling" feature of the invention provides a mechanism where, after initiation of a data transfer, the transferor device may suspend an on-going data transfer. For example, page 12, lines 3-13 of the application states:

> A transfer can be stalled by the transferor by driving the link status line in accordance with the link bus protocol. The protocol establishes a window in which pacing status information may be driven onto the link bus status line. In an exemplary embodiment, the transferor may stall the transfer by initially driving the status line low during the window. The protocol also establishes that after the transfer has been stalled, the transferor should drive the status line high before tristating on the next clock cycle. As noted earlier, a pull-up device is connected to the status line, which substantially guarantees stable status information during turn-around times on the status signal. When no data stall is to occur, the pull-up device may be sampled instead of actively driving the status line, which has the effect of speeding up the turn-around cycle.

The "null response" of the AStatIn/AStatOut is equated by the Final Rejection to correspond to the claimed stall feature. In fact, the "null response," as indicated on Blackmon's Table I, merely corresponds to one of four priority levels which can be asserted by bus devices in Blackmon's system. The use of a null response is described, for example, at column 5, line 61 to column 6, line 21, in the context of describing "a command ... issued by a processor ... to store data [at] a memory location via a memory controller," and is in fact directed to part of a method for initiating a data transfer by a

transferor, and thus wholly unrelated to stalling an ongoing data transfer, as recited in the claims. Accordingly, there is no disclosure or suggestion in Blackmon regarding the "stalling" features of the claimed invention.

For these reasons, Blackmon cannot be fairly stated to disclose or suggest the invention recited in the above quoted portions of the independent claims.

Additionally, with respect to claims 1-35, Appellant notes the final rejection merely states at page 6 that "one using the device of Blackmon et al. would have performed the same steps set forth in claims 1-35." It is respectfully asserted in making such a statement the Final Rejection has failed to make a prima facia case of unpatentability, as the depending claims of recite additional limitations which the Final Rejection has not specifically addressed. Claims 2-17, 19, 21-29, 31-35, 38-46, 50-55, 57-59, and 62-64 recite further elements of the link bus protocol of the invention. The Final Rejection has not specifically identified how these limitations are taught or suggested by Blackmon.

Houg is discloses a method and apparatus for obtaining status information. Referring to Fig. 5, the Final Rejection alleges that Houg discloses system 500 including a processor 502, a link hub 506, a satellite device 400, and a link bus 504. This conclusion is in error. As plainly evident in Fig. 5, reference numeral 506 is associated with a bridge circuit for bridging between a processor bus (coupling to processor 502), a memory bus (coupling to RAM 508), a AGP port (coupling to AGP device 510), and a PCI bus 504 (coupling to PCI devices, including devices 512 and target device 400). The PCI bus cannot be a link bus because it is not a point-to-point bus. Simply put, Houg fails to disclose or suggest recited link bus and hub. Houg also fails to disclose or suggest stalling a data transfer. Houg therefore cannot be fairly stated to disclose or suggest the invention recited in the above quoted portions of the independent claims.

Neither Blackmon nor Houg disclose or suggest the recited link bus and hub. Neither Blackmon nor Houg disclose or suggest the recited data stalling feature. Accordingly, no combination of the teachings of Blackmon and Hough would yield the claimed invention.

Independent claims 1, 18, 20, 30, 37, 56, and 65 are believed to be allowable over the prior art of record. The depending claims (i.e., claims 2-17, 19, 21-29, 31-36, 38-55, 57-64, and 66-69) are also believed to be allowable for at least the same reasons as the independent claims.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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